Tutorial, Hot Chips Conference
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Morning Session

MOSFET and Front-End Process Integration: Scaling, Challenges, and Potential Solutions Through the End of the Roadmap

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INTERNATIONAL SEMATECH

Outline

- Introduction/ITRS
- MOSFET scaling and its impact
- Front-end approaches and solutions
- Non-classical CMOS
- Conclusions

Introduction

- **IC technology: following Moore's Law by rapidly scaling into deep submicron regime (currently, 130nm technology generation)**
  - Increased speed
  - Lower power dissipation per function
  - Increased transistor and function density
  - Lower cost/function
- **The scaling results in major MOSFET and process integration issues, including**
  - Simultaneously maintaining satisfactory I_{on} (drive current) and I_{leak}
  - High gate leakage current for very thin gate dielectrics
  - Fabrication and control of very abrupt, shallow, low sheet resistance S/D extensions
  - Control of short channel effects for very small transistors
  - Etc.
- **Potential solutions & approaches:**
  - Material and process (front end): high K gate dielectric, metal gate electrodes,…
  - Structural: non-classical CMOS device structures

International Technology Roadmap for Semiconductors (ITRS)

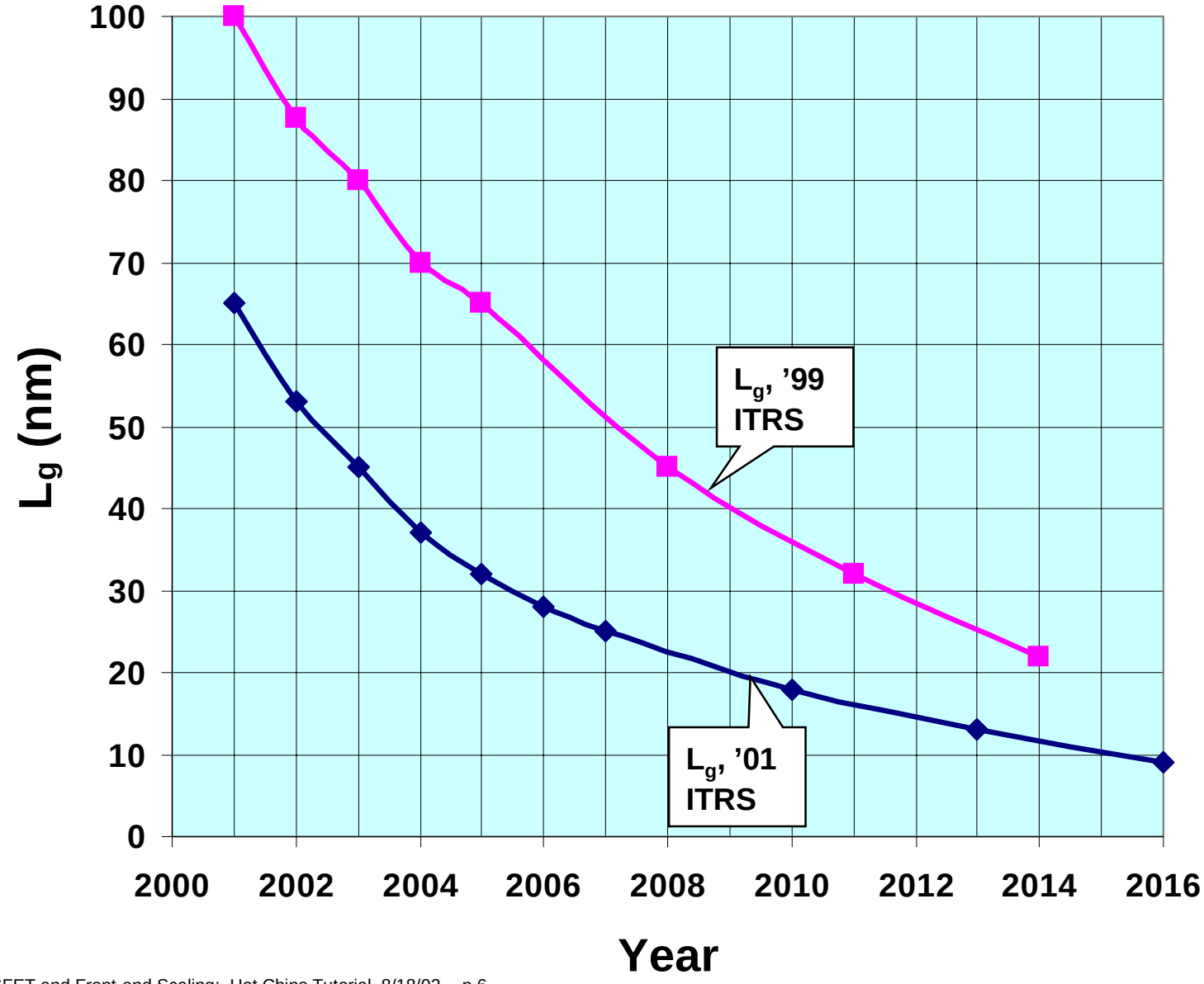
- **Industry-wide, fully international effort to map IC technology generations for the next 15 years**
  - For each technology generation
    - Projects targets for technology characteristics and requirements
    - Assesses key needs and gaps
    - Lists potential solutions
  - Provides common reference for semiconductor industry: device manufacturers, equipment and materials vendors, researchers
    - Is not meant to restrict research, pick winners
      - Focus: stimulating needed R&D
    - Useful for planning
  - Enabling factor in continuing to follow Moore's Law
  - Most of projections in this talk from 2001 ITRS

Key Overall Chip Parameters for High-Performance Logic, from 2001 ITRS

		Near Term							Long Term		
Calendar Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM Half Pitch	nm	130	115	100	90	80	70	65	45	35	22
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Maximum on-chip local clock frequency	GHz	1.7	2.3	3.1	4.0	5.2	5.6	6.7	11.5	19.4	28.8
Allowable maximum power dissipation, with heatsink	W	130	140	150	160	170	180	190	218	215	288
Number of transistors per chip	Millions of transistors	276	348	439	553	697	878	1106	2212	4424	8848

- The DRAM half pitch and L_g are drivers of IC technology scaling, including lithography (to be discussed by Prof. Wong)
- Technology generations (in red) defined by DRAM half pitch
  - This is a dense feature: drives functional density
  - –Reduction factor of 0.7X ~ 1/• 2 between generations (130nm in 2001, 90nm in 2004, 65nm in 2007, etc.)h
  - –Three years between generations
- –Gate length (L_g) ≤ 0.5 X DRAM half pitch
  - –These are isolated features
  - –Rapid scaling of L_g is driven by need to improve transistor speed

2001 vs. 1999 ITRS Projections of Physical Gate Length (L_g): High Performance Logic



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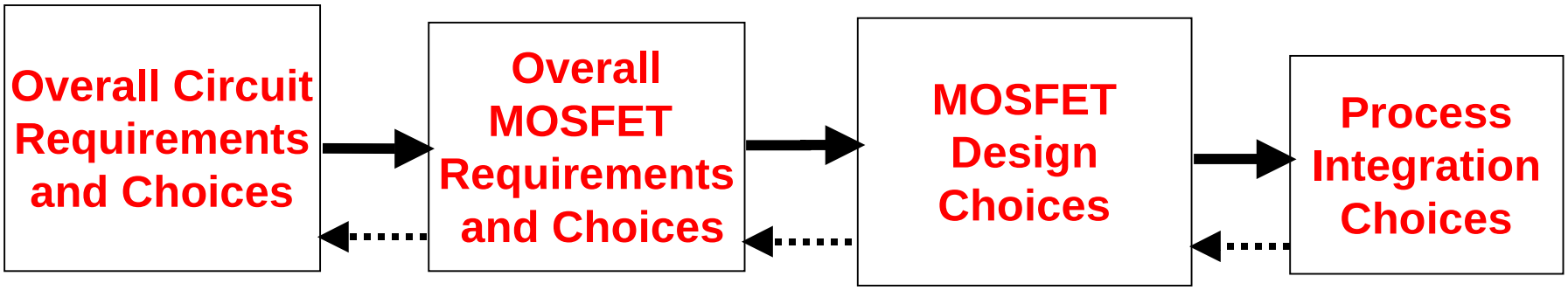
Hierarchy of IC Requirements and Choices



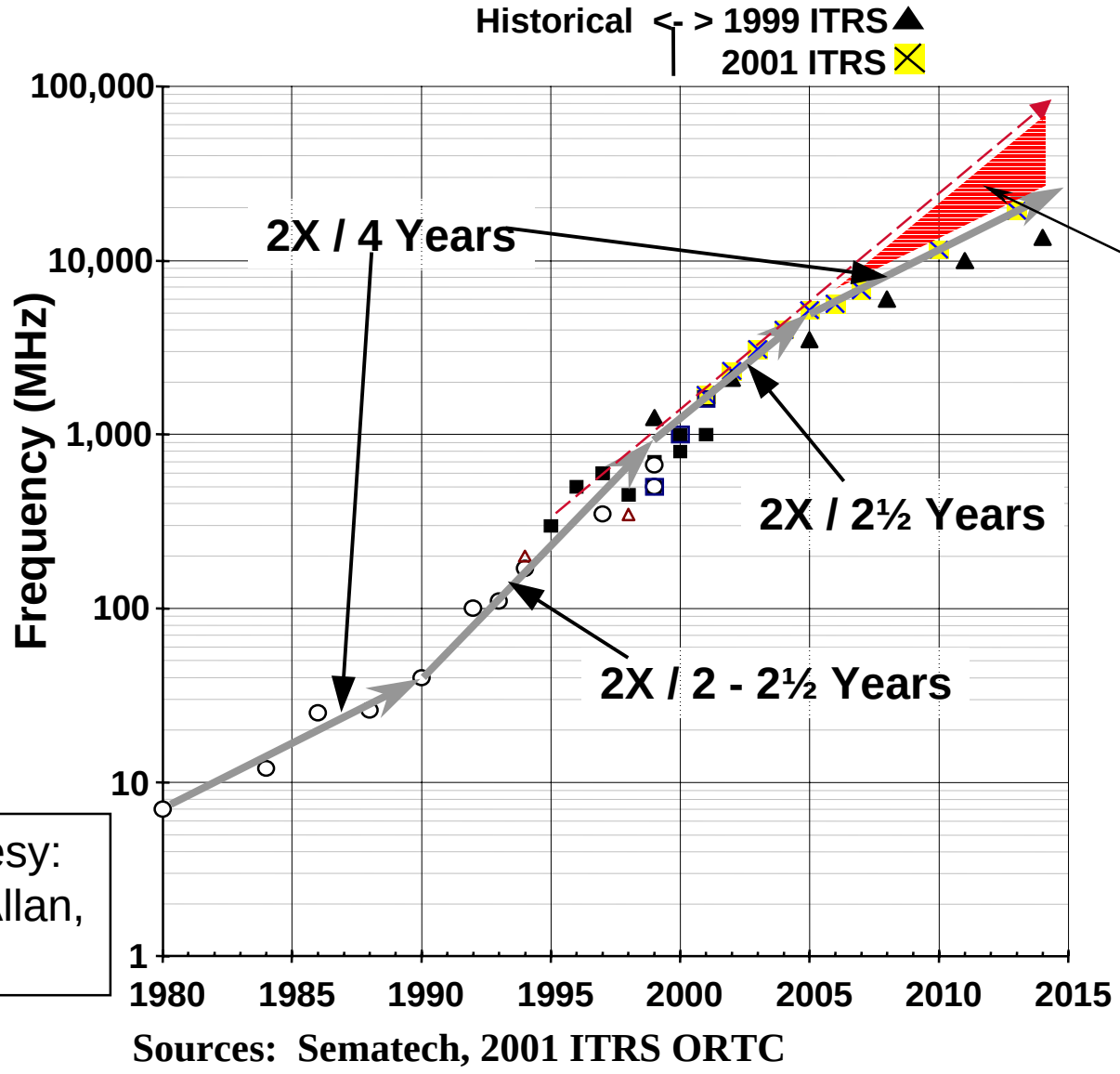
- Chip Power
- Chip Speed
- Functional Density
- Chip Cost
- Architecture
- Etc.

- V_{dd}
- MOSFET Leakage
- MOSFET Drive current
- Parasitic series resistance
- Transistor size
- V_t control
- Reliability
- Etc.

- T_{ox}, L_g, x_j, R_s
- Channel engineering
- Oxynitride or High K gate dielec.
- Classical Planar Bulk or Non-classical CMOS Structures
- Etc.

- Thermal processing
- Overall process flow
- Process modules
- Material properties
- Boron penetration
- Etc.

Historical Data and ITRS Projections for Chip Clock Frequency, High-Performance Logic



Sources: Sematech, 2001 ITRS ORTC

Courtesy: Alan Allan, Intel

Actual Scaling Acceleration, Or Equivalent Scaling Innovation Needed to maintain historical trend

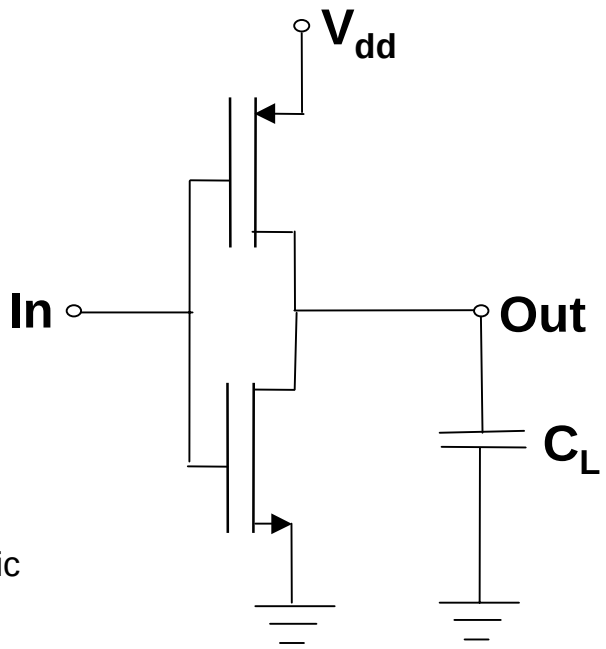
MPU Clock Frequency Historical Trend:

Gate Scaling, Transistor Design contributed ~ 17-19%/year

Architectural Design innovation contributed additional ~ 21-13%/year

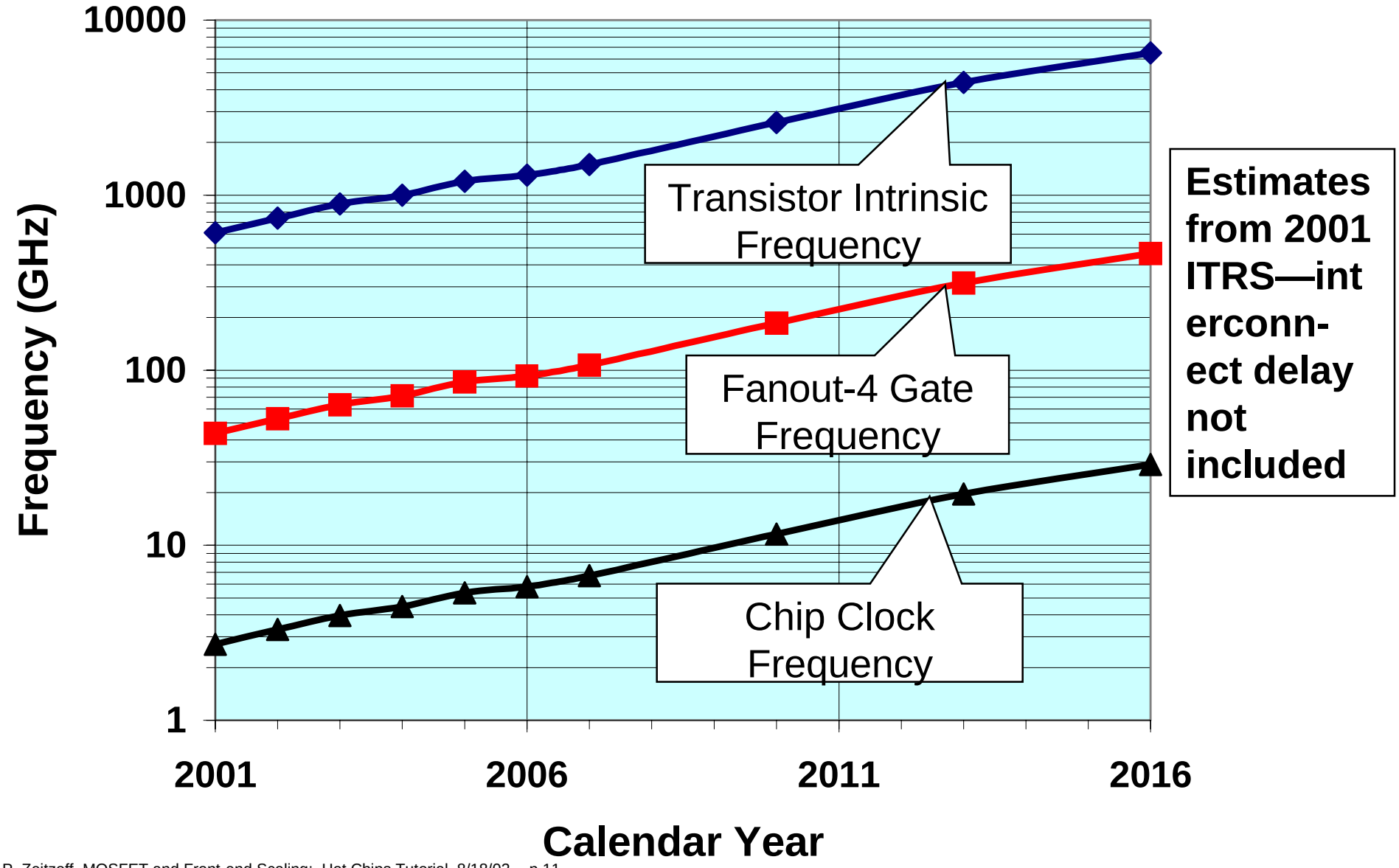
Impact of Key MOSFET Parameters on Circuit Performance

- **Transistor intrinsic delay, τ**
  - $\tau \sim C\ V_{dd}/(I_{on}*W)$
    - I_{on} units: μA/μm
    - $C = C_{s/d} + C_L$
      - Gate dominated (local, dense logic)
        - $C \sim C_L = C_{gate} \sim C_{ox}*W*L_g + C_{parasitic}$
        - $C_{ox} \sim \varepsilon_{ox}/T_{ox}$
      - Interconnect dominated (long leads): $C \sim C_L \sim C_{metal}$
        - We won't consider this case: Mike Thomas will cover it in Interconnect lecture



- **Transistor intrinsic switching frequency = $1/\tau$**
  - **Good metric for transistor performance**
  - **To maximize $1/\tau$, maximize I_{on}**

Frequency scaling: Transistor Intrinsic (1/τ), Fanout-4 Gate, Chip Clock



ITRS Drivers for Different Applications

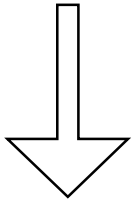
- **High performance chips (MPU, for example)**
  - Driver: maximize chip speed→maximize transistor performance
    - Goal of ITRS scaling: $1/\tau$ increases at ~ 17% per year, historical rate
      - Must maximize I_{on}
      - Consequently, I_{leak} is relatively high
- **Low power chips (mobile applications)**
  - Driver: minimize chip power→minimize I_{leak} (to conserve battery power)
    - Goal of ITRS scaling: specific, low level of I_{leak}
    - Consequently, $1/\tau$ is considerably less than for high-performance logic

Device Scaling Approach: 2001 ITRS

- **Simple models capturing essential MOSFET physics→embedded in a spreadsheet**
  - Initial choice of scaled MOSFET parameters is made
  - Using spreadsheet, MOSFET parameters are iteratively varied to meet ITRS targets
    - High Performance: 17%/year increase in $1/\tau$
    - Low Power: specific, low level of leakage current

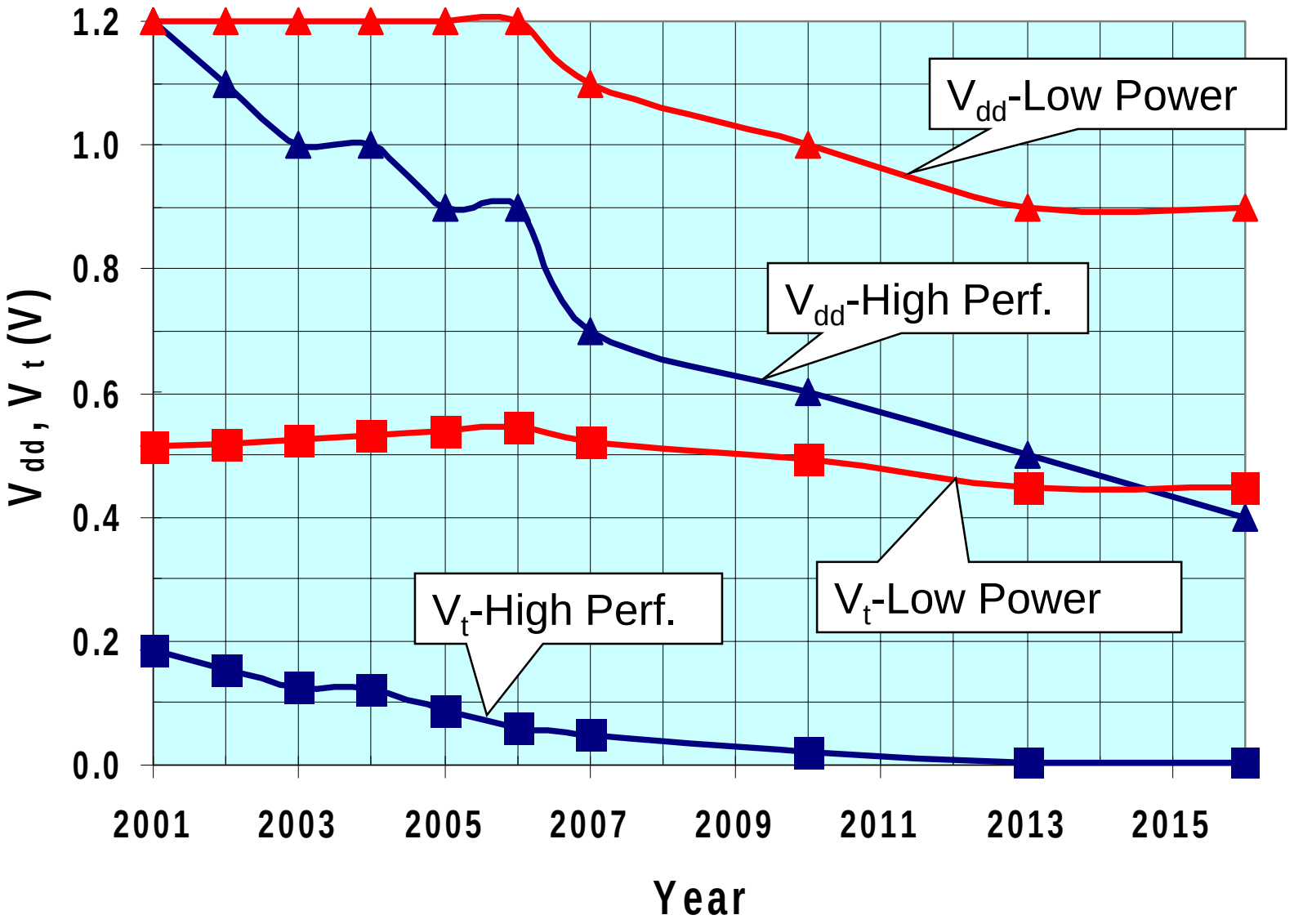
V_{dd} and V_t Device Scaling Issues

- **Preference: scale V_{dd} down rapidly with tech. generations**
  - To keep dynamic power dissipation (~V_{dd}^2) within acceptable bounds
  - For reliability, control of short channel effects (SCE), general device scaling
- **$1/I_{sd,leak}$ exp. dependent on V_t**
- **I_{on} strongly dependent on gate overdrive, (V_{dd}-V_t)**

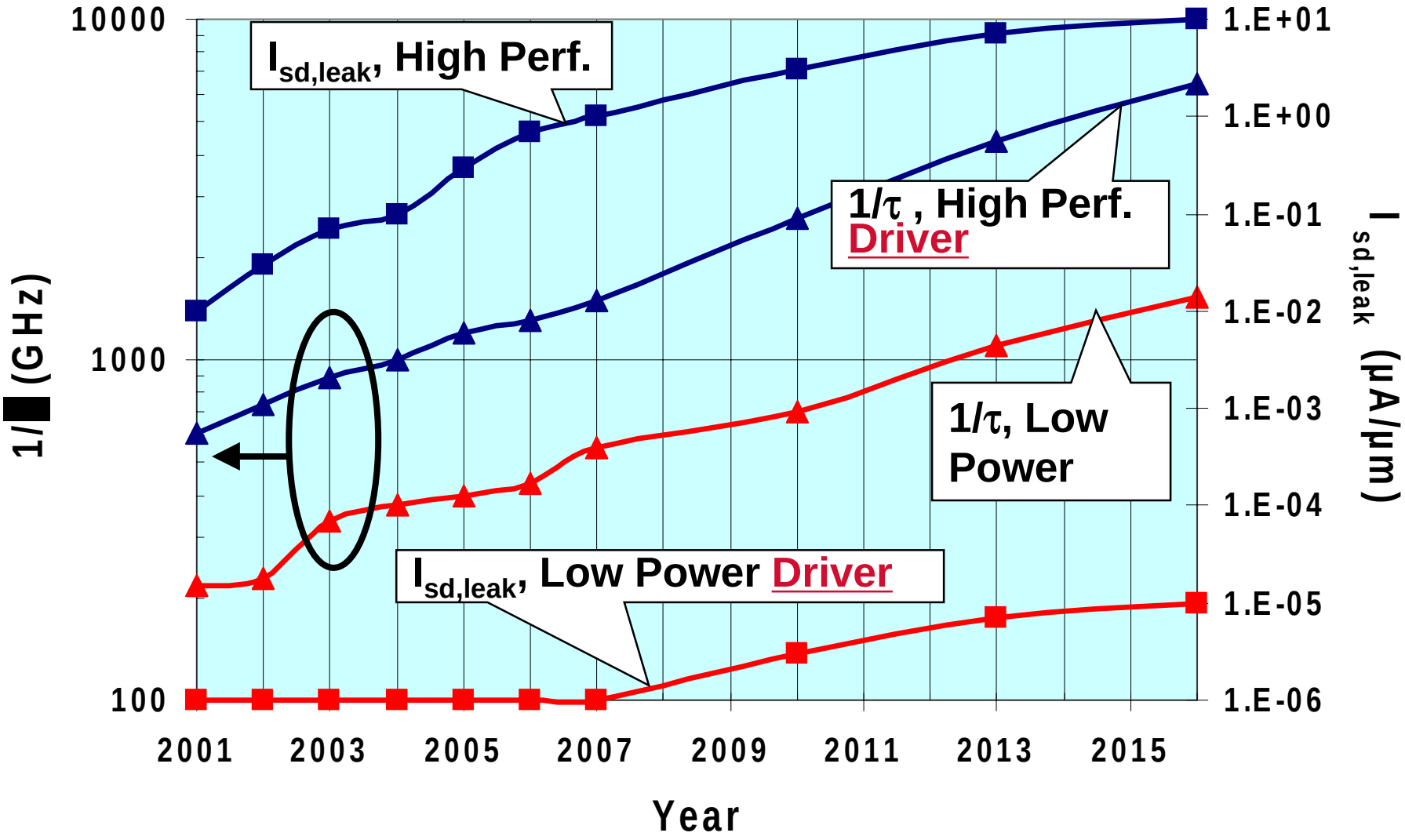


- **Difficult tradeoffs between I_{on} and $I_{sd,leak}$, V_{dd} and V_t with scaling**

ITRS Projections of V_{dd} and V_t Scaling



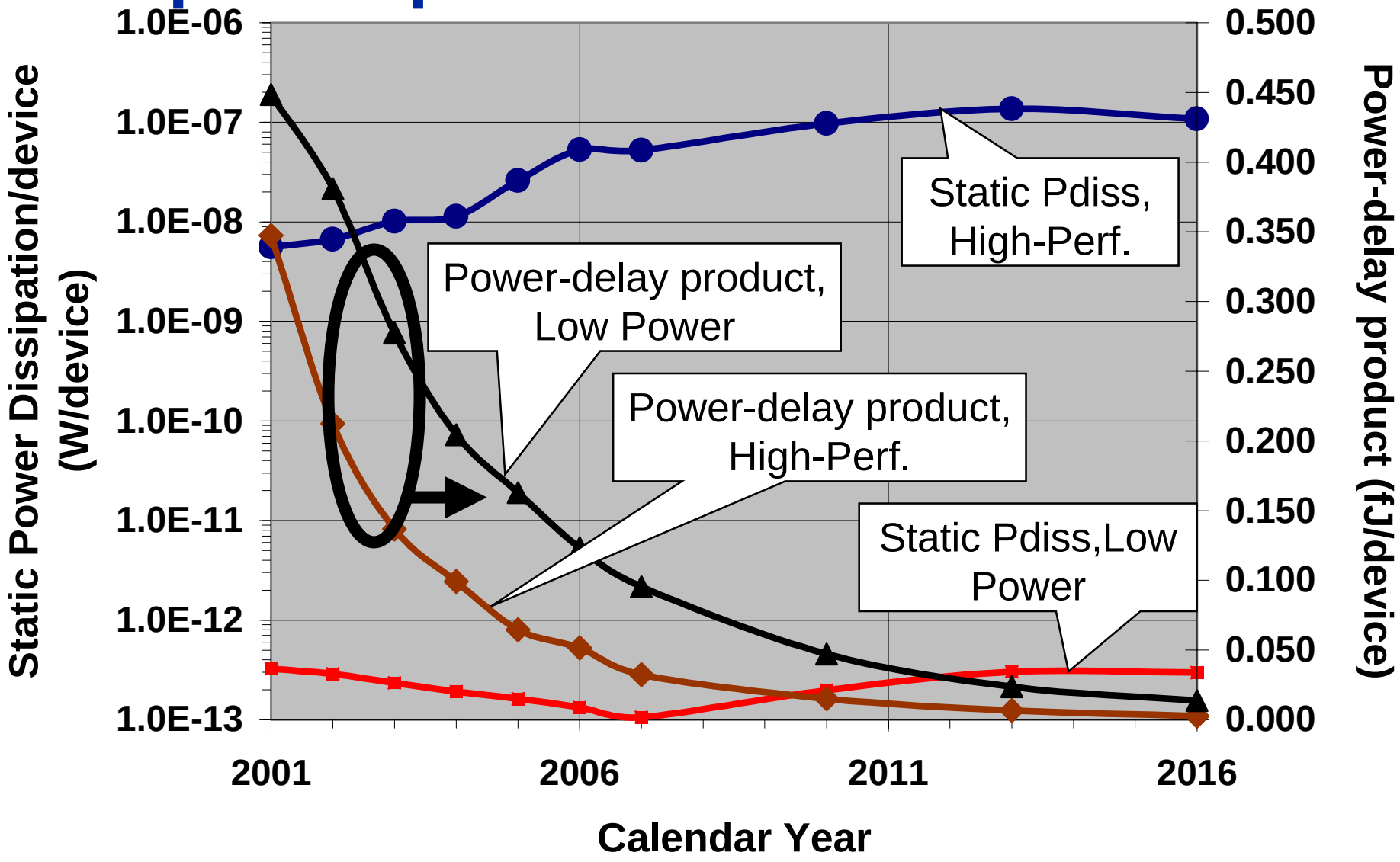
ITRS Projected Scaling of $1/\tau$ and $I_{sd,leak}$ for High Performance and Low Power



Key MOSFET Scaling Results

- High-performance logic
  - **Average 17%/yr improvement in $1/\tau$ is attained**
  - **$I_{sd,leak}$ is very high, particularly for 2007 and beyond ➔ chip static power dissipation scaling is an issue**
    - **Assumption: $I_{gate} \leq I_{sd,leak}$ ➔ uncomfortably large I_{gate}**
- Low-power logic
  - **Very low $I_{sd,leak}$ target is met**
    - **$I_{gate} \leq I_{sd,leak}$ ➔ I_{gate} is very low: difficult to meet this**
  - **$1/\tau$ scales considerably slower than for high-performance**

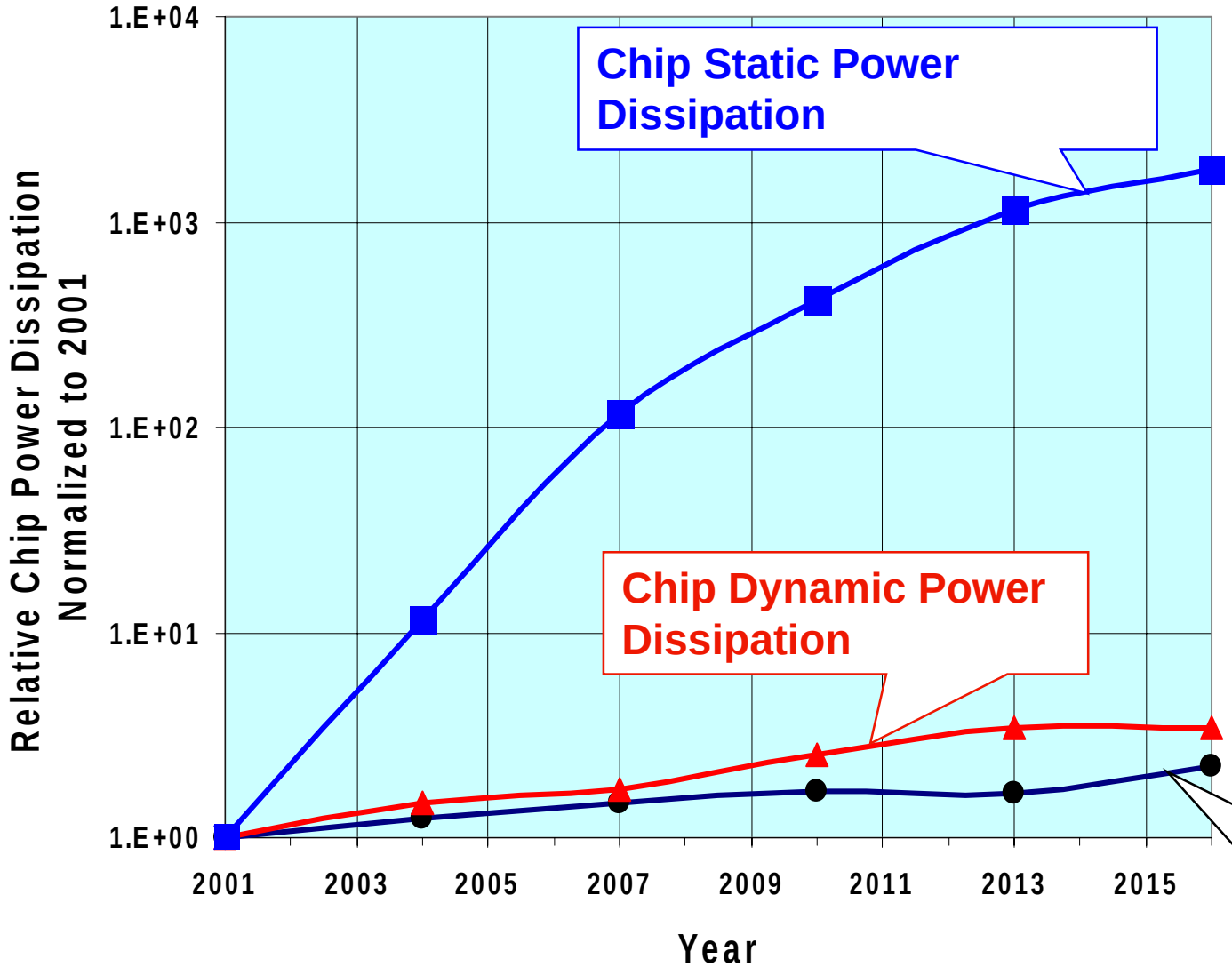
ITRS Projected Scaling of Power Dissipation per Device



Impact of Key MOSFET Parameters on Chip Power Dissipation

- **$P_{total} = P_{dynamic} + P_{static}$**
  - $P_{dynamic} = C_{active} V_{dd}^2 f_{clock}$
    - With scaling, C_{active} and f_{clock} increase rapidly
    - **To keep $P_{dynamic}$ within tolerable limits, reduce V_{dd} with scaling**
    - Reduce V_{dd} for reliability, SCE, general device scaling reasons, also
  - $P_{static} = N_{off} W I_{leak} V_{dd}$
    - With scaling, N_{off} increases rapidly, but V_{dd} and W scale down
    - **To keep P_{static} within tolerable limits, constrain increase of I_{leak} with scaling**

Relative Chip Power Dissipation per ’01 ITRS, High Performance



Assumptions:

- **Only one type of (high I_{on}, high I_{leak}) transistor, and no power reduction techniques.**
- **Simple scaling**
- **This is an unrealistic scenario, only meant to clearly illustrate static power dissipation issues**

Potential Solutions for Power Dissipation Problems, High-Performance Logic

- **Increasingly common approach: multiple transistor types on a chip→multi-Vt, multi-Tox, etc.**
  - **Only utilize high-performance, high-leakage transistors in critical paths—lower leakage transistors everywhere else**
  - **Improves flexibility for SOC**
- **Electrical or dynamically adjustable Vt devices (future possibility)**
- **Circuit and architectural techniques: pass gates, power down circuit blocks, etc.**

Summary: MOSFET Scaling

- **MOSFET scaling is the "raw material" for designers to improve chip performance, control power dissipation**
  - **MOSFET scaling has historically contributed ~17% per year in "raw" speed improvement for high-performance logic**
  - **Design and architectural innovation has contributed about as much**
- **MOSFET scaling goals are critically important**
  - **High-performance logic emphasizes speed at the expense of high leakage and static power dissipation**
  - **Low-power logic emphasizes low leakage at the expense of speed**
  - **Dialogue between designers and technologists is essential**
- **Static power dissipation is a growing problem for high-performance logic, and there are numerous approaches to dealing with it, esp. including design**

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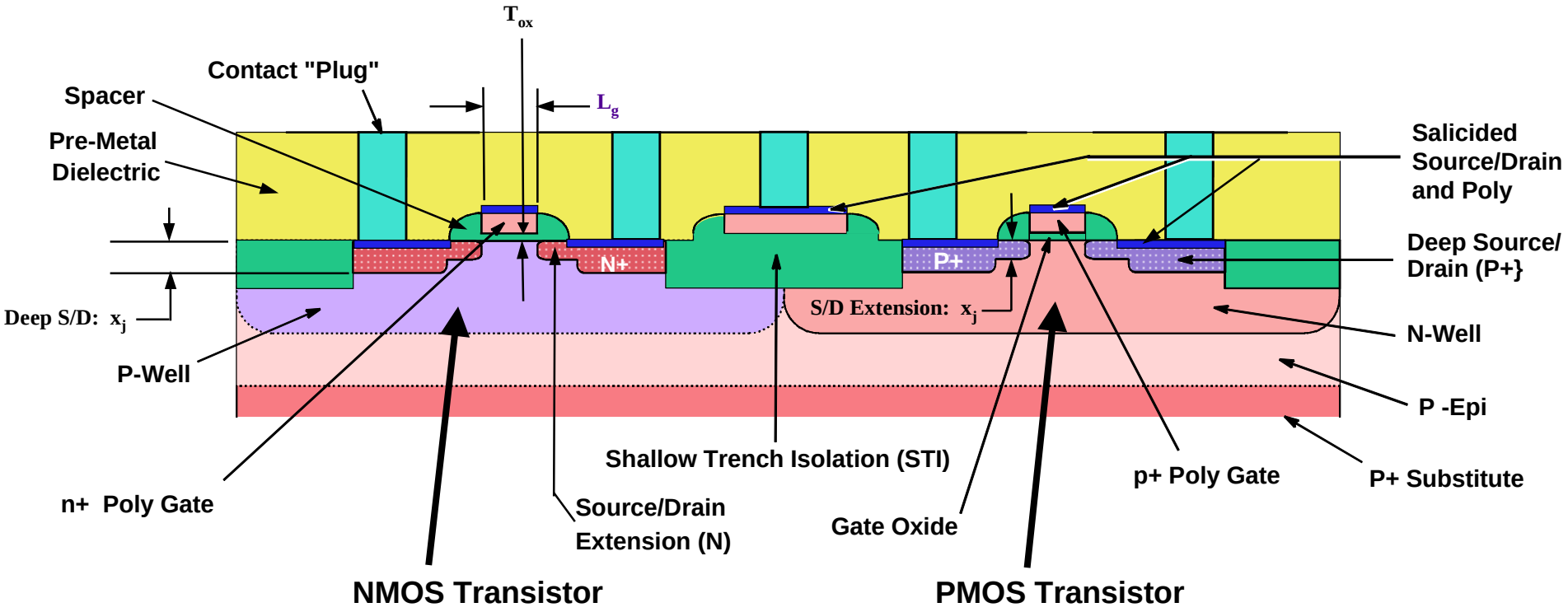
Simplified Cross Section of a Typical PMOSFET and NMOSFET

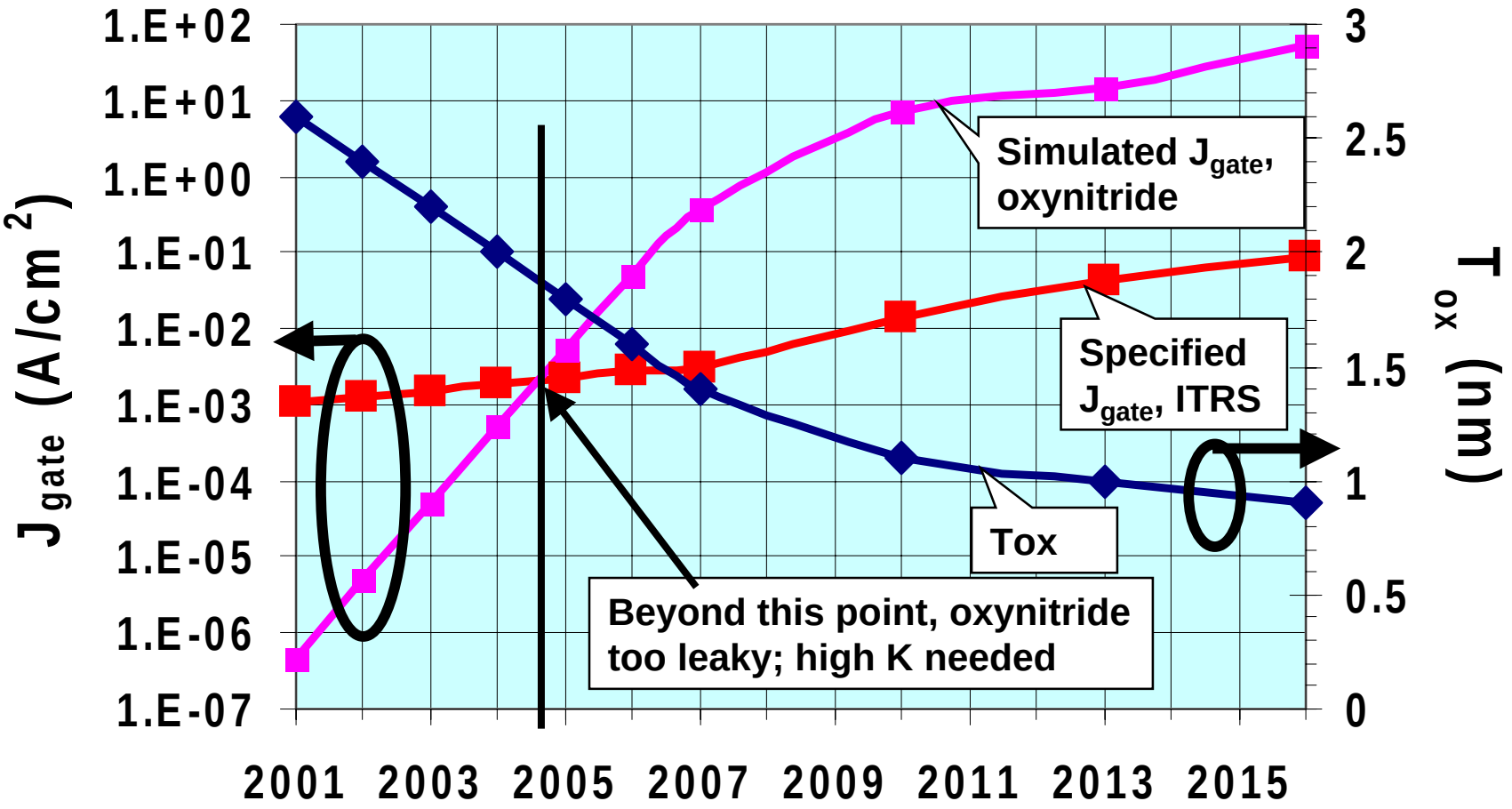
(Not to scale)



Difficult Transistor Scaling Issues

- **Previously discussed scaling results involve high-level, idealized MOSFET physics**
  - **Assumption: highly scaled MOSFETs with required characteristics can be successfully fabricated**
- **All lateral and vertical MOSFET dimensions (T_{ox}, x_j's, spacer width, etc.) are scaling down rapidly along with L_g**
- **With scaling, increasing difficulty in meeting transistor requirements**
  - **High gate leakage**
    - **Direct tunneling increases rapidly as T_{ox} is reduced**
  - **Poly depletion in gate electrode→increased effective T_{ox}, reduced I_{on}**
  - **Scaling S/D extension: x_j – ρ_{s-}→high $R_{series,s/d}$, reduced I_{on}**
  - **Etc.**

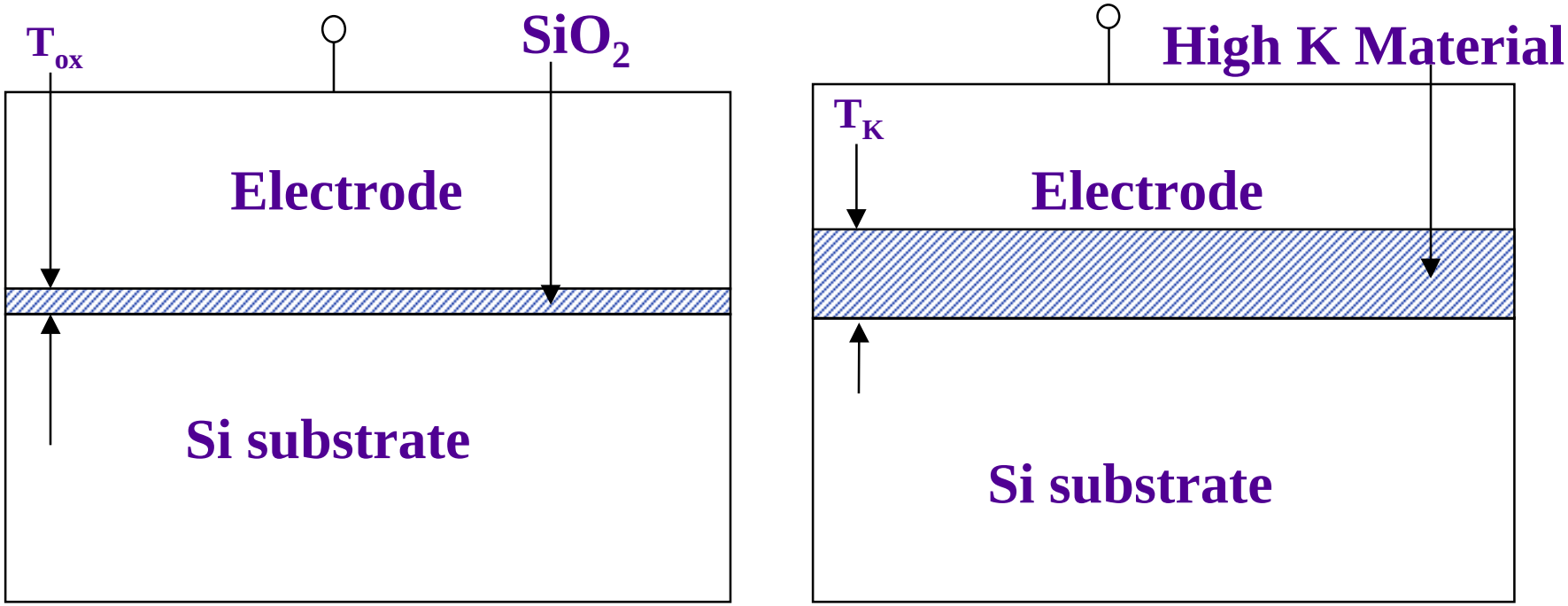
2001 ITRS Projections Versus Simulations of Direct Tunneling Gate Leakage Current Density for Low Power Logic



(Simulations courtesy of C. Osburn, NCSU and ITRS)

Implementation of high K will be driven by Low Power Logic in 2005

High K Gate Dielectric to Reduce Direct Tunneling



- **Equivalent Oxide Thickness = EOT = T_K * (3.9/K) = T_{ox}, where 3.9 is relative dielectric constant of SiO2 and K is relative dielectric constant of high K material**
  - **C = Cox = ε_{ox}/T_{ox}**
  - **To first order, MOSFET characteristics with high-k are same as for SiO2**
- **Because $T_K > T_{ox}$, direct tunneling leakage much reduced with High K**
  - **If energy barrier is high enough**
- **Candidate materials: LaO_2/HfO_2/ (K~15 - 30); Hf, Zr-SiO4 (K~12 - 16); others**

High K Issues

- **Process integration issues**
  - Thermal stability of high K material
    - Conventional flow, with S/D anneal, etc., difficult
      - "Replacement gate" flow is an option
  - Thermal, chemical compatibility with polysilicon, & B penetration
    - Metal electrode may be required
  - Interface with Si substrate
    - Most form thin SiO_2 layer: increases $T_{ox,equiv}$
- **Interface properties: increased surface states, fixed charge density; reduced mobility**
- **Leakage, reliability**
- **SCE→fringe field effects**
- **New material: major challenge**

Difficult Transistor Scaling Issues

- Previously discussed scaling results involve high-level, idealized MOSFET physics
  - Assumption: highly scaled MOSFETs with required characteristics can be successfully fabricated
- All lateral and vertical MOSFET dimensions (T_{ox}, x_j's, spacer width, etc.) are scaling down rapidly along with L_g
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  - Etc.

Polysilicon Limitations

Polysilicon depletion: band bending in the polysilicon

- Increases effective electrical T_{ox} ➔ reduces E_{ox}, & hence inversion charge
- More of a problem as T_{ox} is scaled ➔ Poly doping must increase with scaling
  - Ge-Si might help

- **PMOSFETs: B penetration through very thin oxides**
  - Oxy-nitrides & reduction of DT effective now
- **Compatibility with high K**
- **Gate resistance of very thin gates (even with silicide)**

Metal Gate Electrodes

- **Metal gate electrodes are a potential solution: probably implemented at 65 nm tech. generation (2007) or beyond**
  - **No depletion, very low resistance gate, no boron penetration, compatibility with high-k**
  - **Issues**
    - **Different work functions needed for PMOS and NMOS==>2 different metals needed**
      - **Process complexity, process integration problems**
    - **Etching of metal electrodes**
    - **New materials: major challenge**

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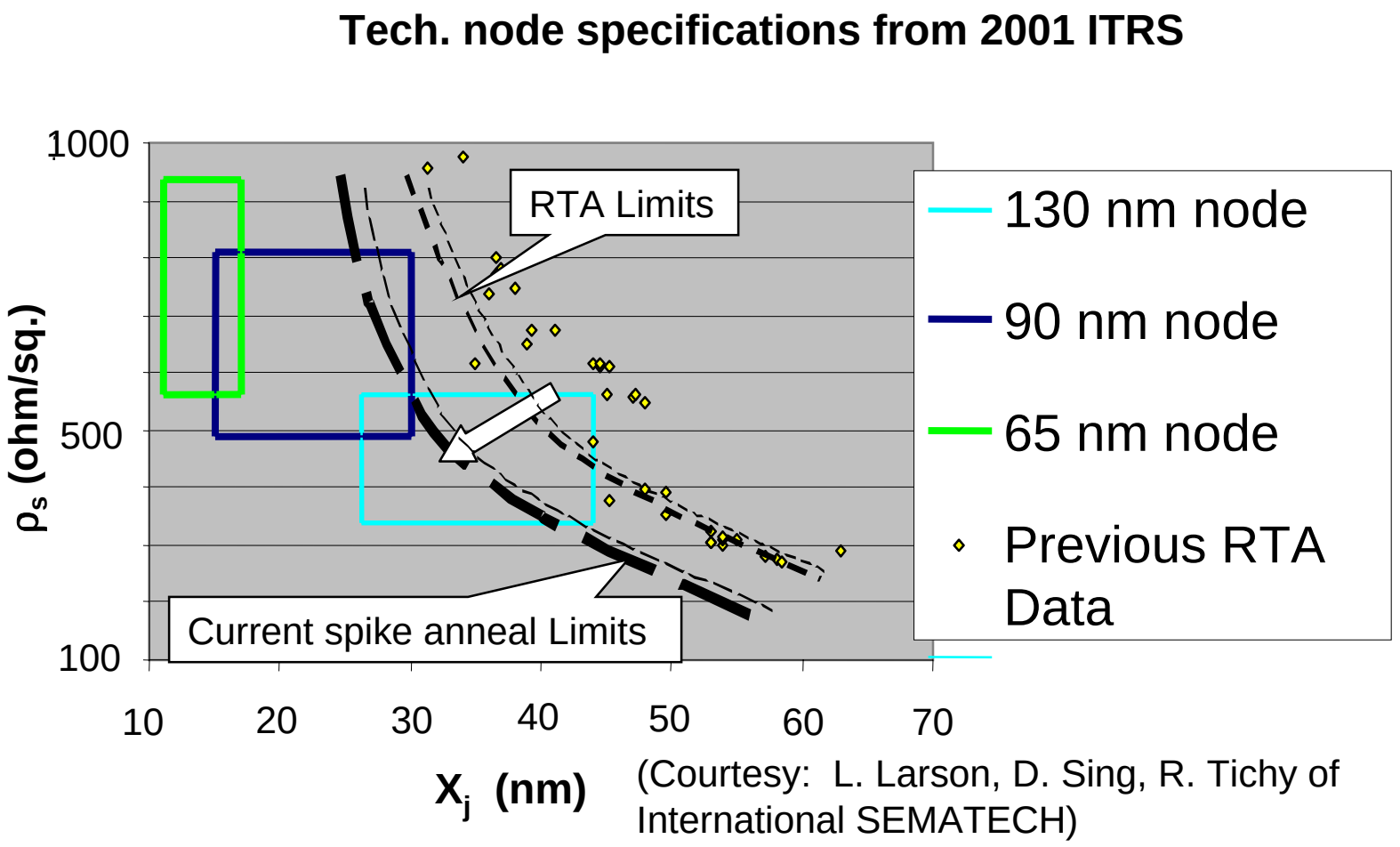
S/D Extension Issues

- **Increasingly abrupt, shallow, heavily doped profiles required for successively scaled technologies**
  - Needed for optimal devices, esp. to control SCE
  - Difficult to fabricate, esp. for PMOS (B)
  - Tends to increase ρ_s ➔ $R_{S/D,series}$
- **Potential solutions**
  - Ultra-low energy implants (< 1 KeV, B)
  - Rapid Thermal Processing (RTP) and spike anneal: reduces DT & TED
  - Increase dose as much as possible==>reduced $R_{S/D,series}$
- **90 nm technology or beyond: novel doping and/or annealing**
  - Laser thermal annealing, etc.
  - Plasma or gas phase doping, etc.
  - Co-implant

S/D Extension Solutions



65 nm node and beyond: may require novel doping and annealing techniques

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Limits of Scaling Planar, Bulk MOSFETs

- **65 nm tech. generation (2007, L_g = 25nm) and beyond: increased difficulty in meeting all device requirements with classical planar, bulk CMOS (even with material and process solutions: high K, metal electrodes, ….)**
  - Control of SCE
  - Impact of quantum effects and statistical variation
  - Impact of high substrate doping
  - Control of series S/D resistance ($R_{series,s/d}$)
  - Need for enhanced mobility, $I_{d,sat}$
  - Others

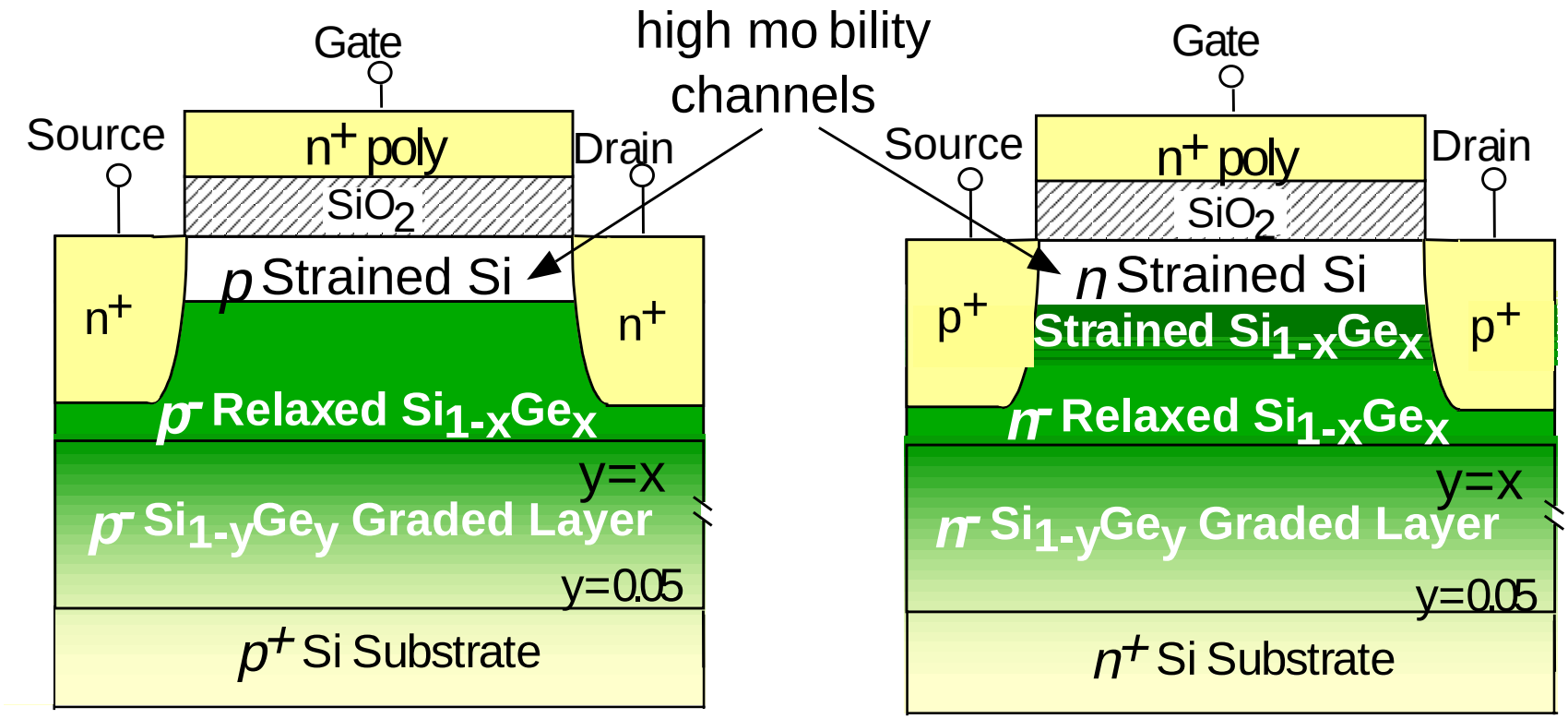
Alternative device structures (non-classical CMOS) may be utilized

- Band engineered transistors→improved transport/mobility
- Ultra thin body SOI
- Double gate SOI - Including FinFET and Vertical FETs.

Technology Requirement Projections for High-Performance Logic from 2001 ITRS: Mobility Enhancement Issue

		Near Term							Long Term		
Calendar Year		**2001**	**2002**	**2003**	**2004**	**2005**	**2006**	**2007**	**2010**	**2013**	**2016**
DRAM half pitch	**nm**	**130**	**115**	**100**	**90**	**80**	**70**	**65**	**45**	**32**	**22**
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Equivalent oxide thickness, T_{ox}	nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Nominal High-Performance NMOS Sub-Threshold Current, $I_{sd,leak}$ (@25C)	uA/um	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Nominal NMOSFET saturation drive current, I	uA/um	900	900	900	900	900	900	900	1200	1500	1500
Required Percent Current-Drive "Mobility/Transconductance Improvement"		0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Parasitic Series S/D resistance, $R_{sd,series}$	ohm-um	190	180	180	180	180	170	140	110	90	80
Parasitic Source/Drain Resistance (Rsd) Percent of Ideal Channel Resistance (Vdd/Idd)		16%	16%	17%	18%	19%	19%	20%	25%	30%	35%
NMOSFET intrinsic transistor switching frequency, $f_i = 1/t_i$	GHz	610	740	890	1000	1200	1300	1500	2600	4400	6500
Energy per (W/Lgate=3) Device Switching Transition (Cgate*(3*Lgate)*V^2)	fJ/Device	0.347	0.212	0.137	0.099	0.065	0.052	0.032	0.015	0.007	0.002
Static Power Dissipation Per (W/Lgate=3) Device	Watts/Device	5.6E-09	6.7E-09	1.0E-08	1.1E-08	2.6E-08	5.3E-08	5.3E-08	9.7E-08	1.4E-07	1.1E-07

Band Engineered MOSFETs: Surface-channel Strained-Si MOSFET Structures

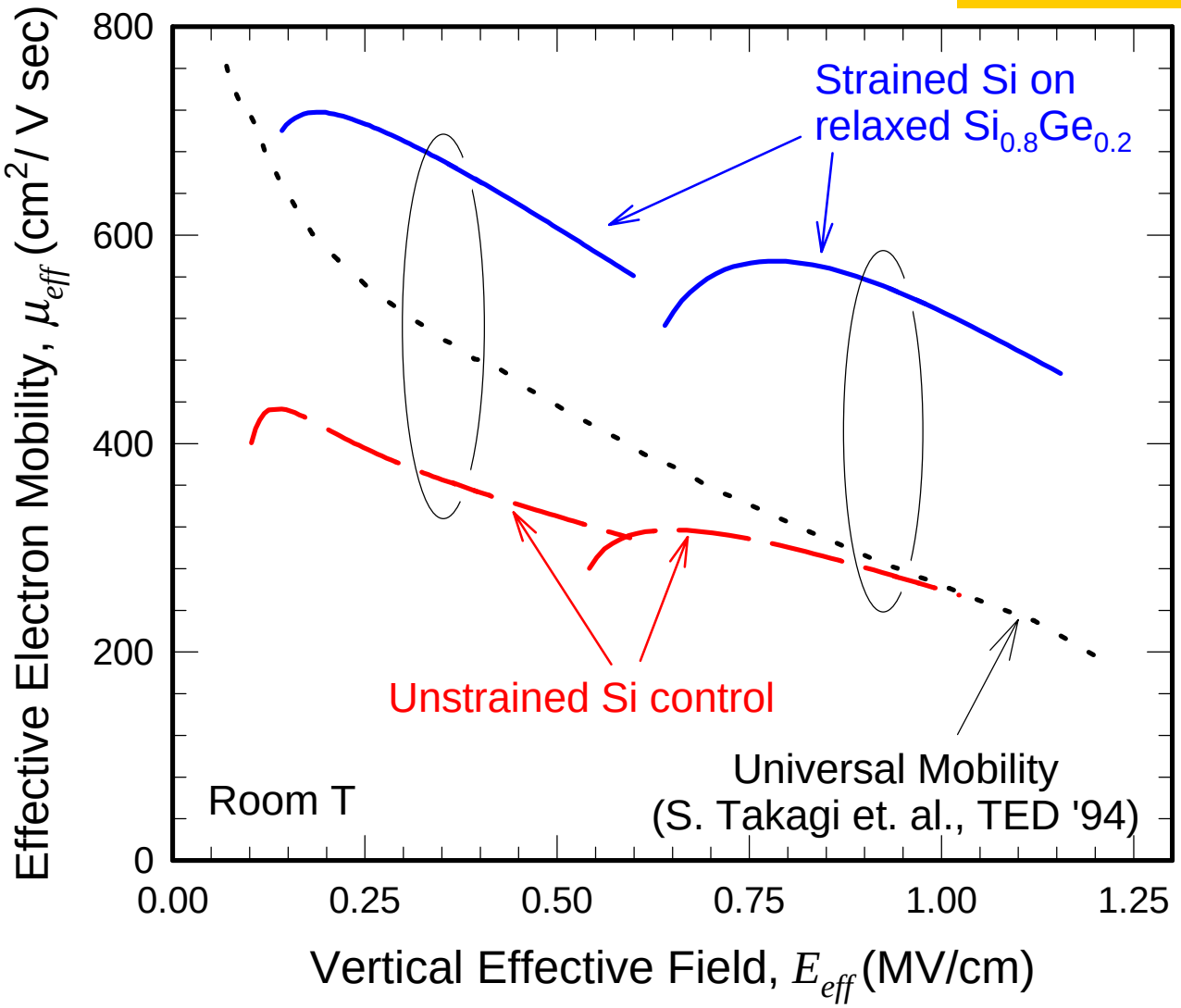


Courtesy of J. Hoyt - MIT

- **+ Increased effective mobility, increased I_{on}**
- **- Difficult integration issues: manufacturability**
- **- Compatibility with ultra-thin body SOI**
- **- Cost**

Electron Mobility Enhancement in Strained Si MOSFETs (Rim.et al.. IEDM 1998)

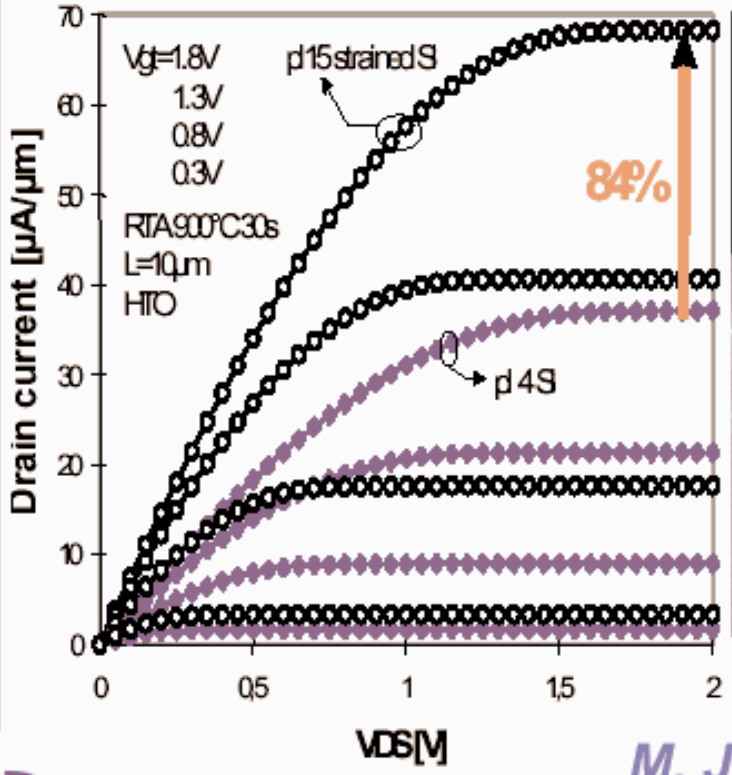
Courtesy of J. Hoyt - MIT

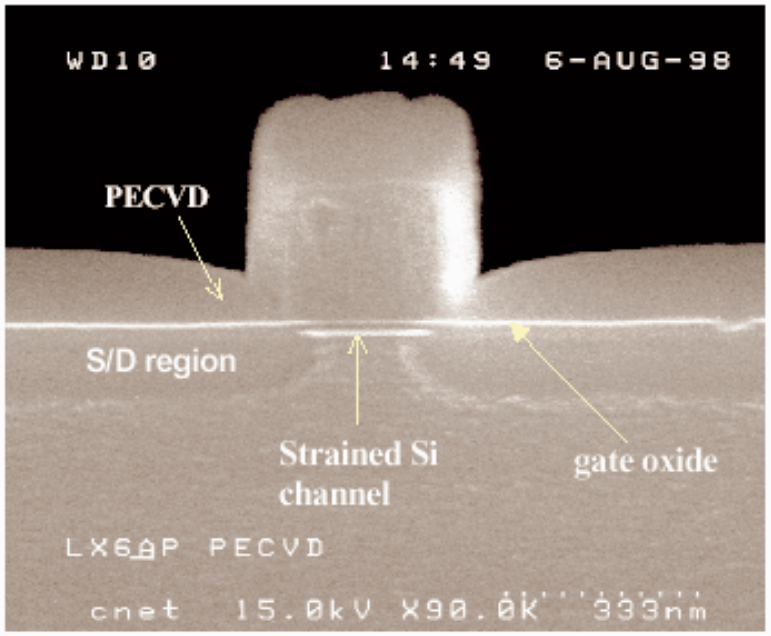


- Electron mobility enhancement of ~ 1.8X persists up to high E_{eff} (~ 1MV/cm)
- Strained-Si allows “moving off” of the universal mobility curve

Strained Si:Ge

HIGH MOBILITY DEVICES - STRAINED Si CHANNELS:





M. Jurczak et al., ESSDERC 1999

SEMI EDUCATION

SEMICON Europa 2001 - Slide 26

Limits of Scaling Planar, Bulk MOSFETs

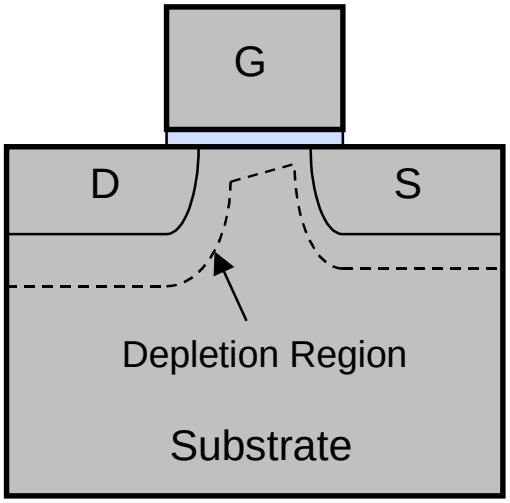
- **65 nm tech. generation (2007, L_g = 25nm) and beyond: increased difficulty in meeting all device requirements with classical planar, bulk CMOS (even with material and process solutions: high K, metal electrodes, ….)**
  - Control of SCE
  - Impact of quantum effects and statistical variation
  - Impact of high substrate doping
  - Control of series S/D resistance ($R_{series,s/d}$)
  - Need for enhanced mobility, $I_{d,sat}$
  - Others

Alternative device structures (non-classical CMOS) may be utilized

- Band engineered transistors→improved transport/mobility
- Ultra thin body SOI
- Double gate SOI - Including FinFET and Vertical FETs.

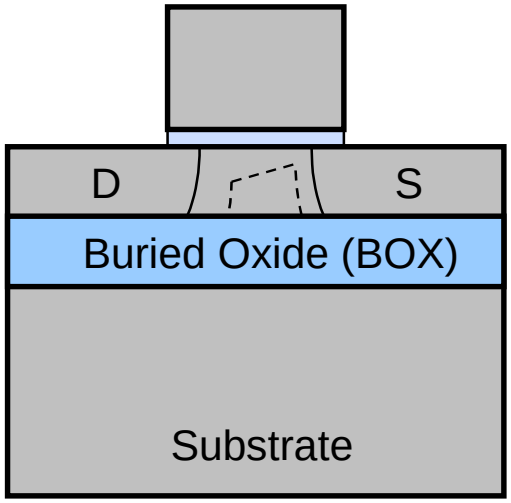
Transistor Structures

Planar Bulk



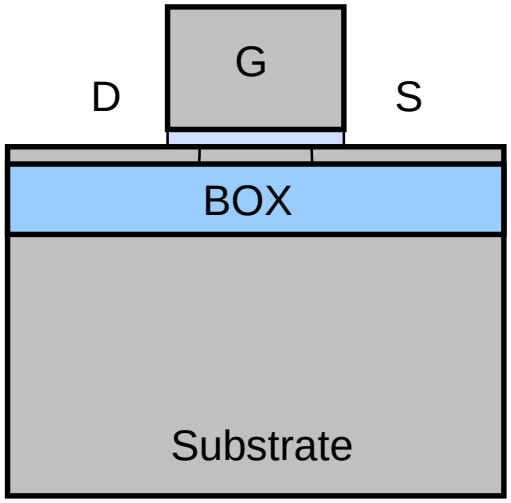
+ Wafer cost / availability
- SCE scaling difficult
- High doping effects and Statistical variation
- Parasitic junction capacitance

Partially Depleted SOI



+ Lower junction cap
+ F.B. performance boost
- F.B. history effect
- SCE scaling difficult
- Wafer cost/availability

Fully Depleted SOI

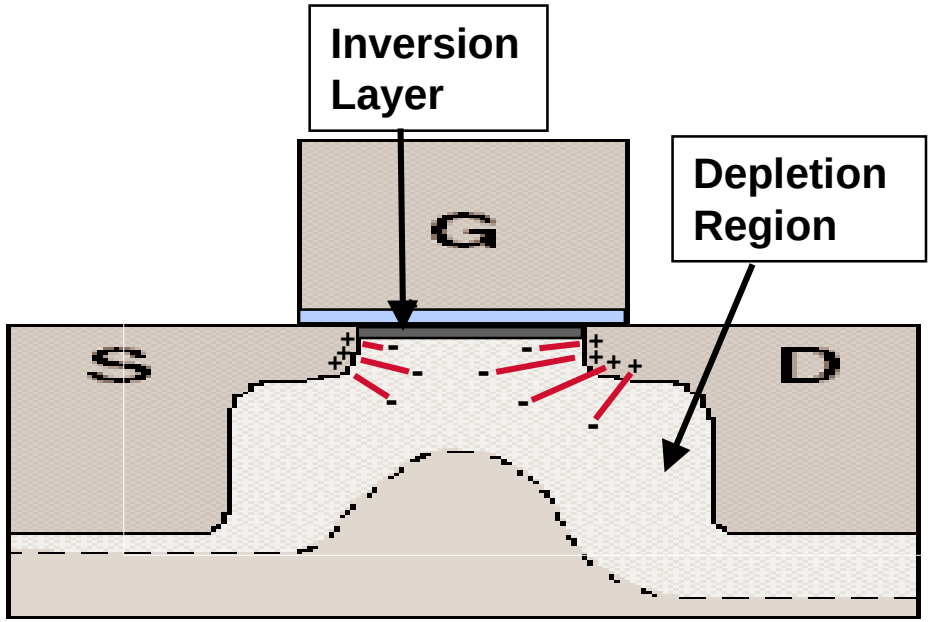


+ Lower junction cap
- SCE scaling difficult
- Increased S/D resistance
- Sensitivity to Si thickness (very thin)
- - Wafer cost/availability

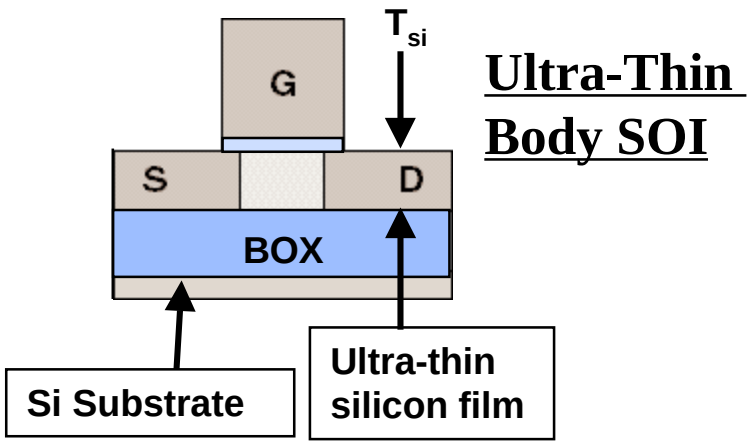
References:

1. P. Zeitzoff, J. Hutchby and H. Huff, to be pub. in Internat. Jour. Of High Speed Electronics and Systems
2. Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

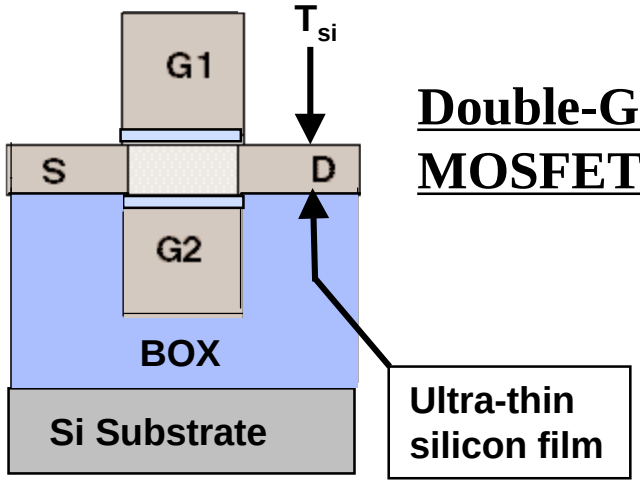
Schematic cross section of planar bulk, UTB SOI, and DG SOI MOSFET



Bulk MOSFET



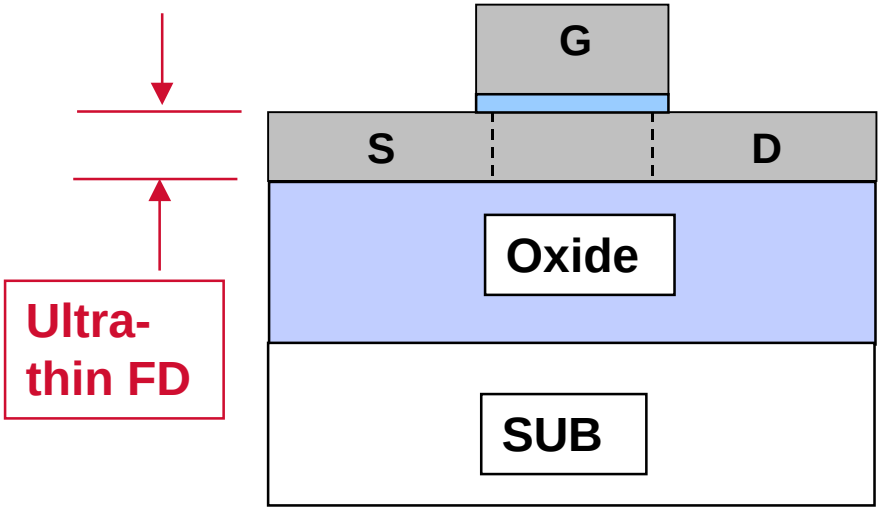
Ultra-Thin Body SOI



Double-Gate SOI MOSFET

Double Gate Transistors

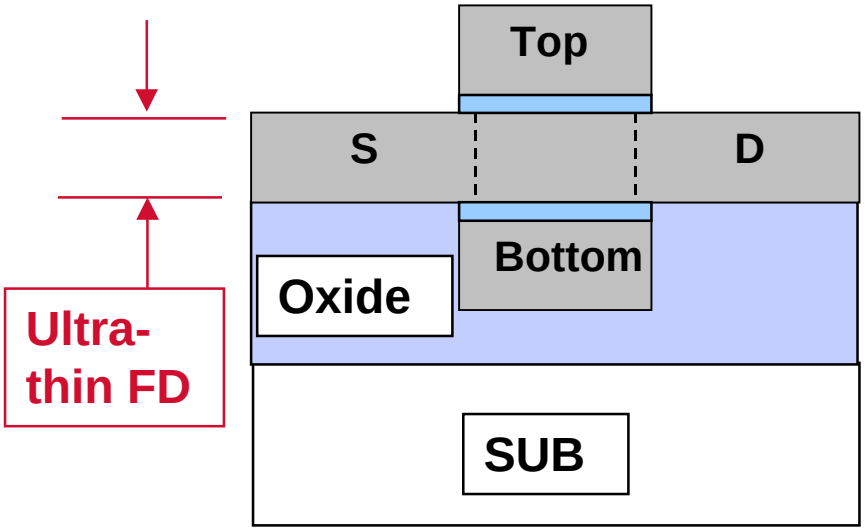
Single Gate:



References:
1. P. Zeitzoff, J. Hutchby and H. Huff, to be pub. in Internat. Jour. Of High Speed Electronics and Systems

2. Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

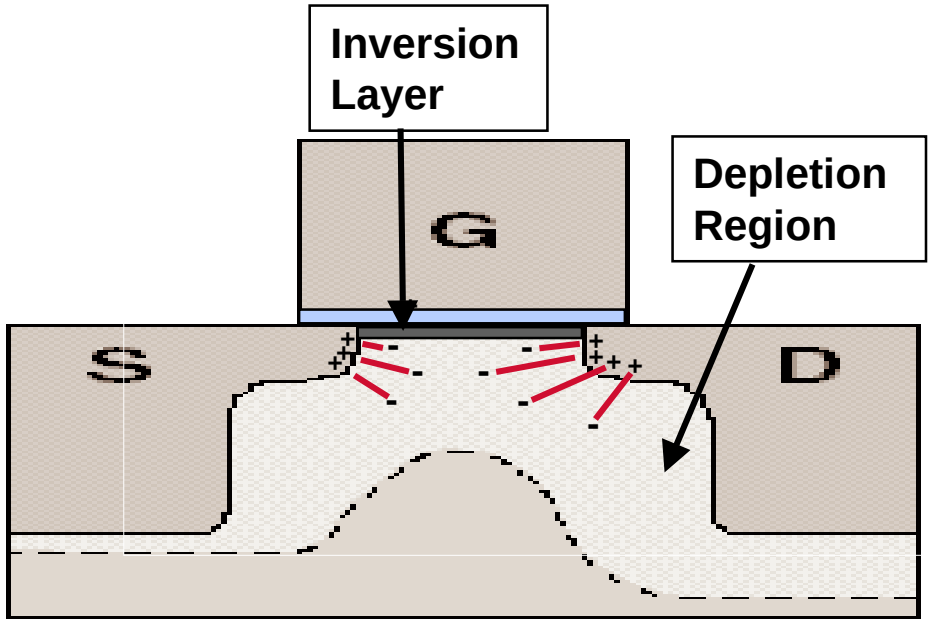
Double-Gate SOI:



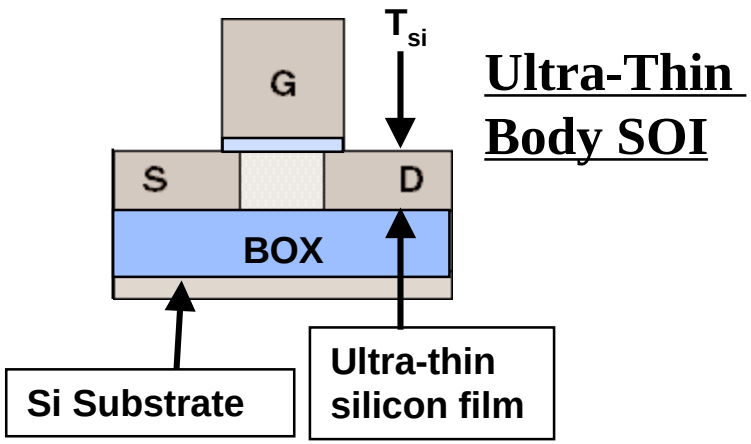
+ ***Enhanced scalability***
+ **Lower junction capacitance**
+ **~2x drive current**
- **~2x gate capacitance**
- **Complex process**

Summary: most advanced, optimal device structure, but difficult to fabricate

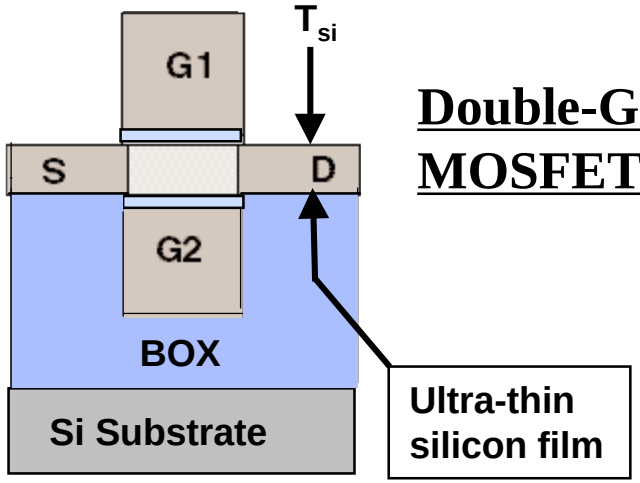
Schematic cross section of planar bulk, UTB SOI, and DG SOI MOSFET



Bulk MOSFET



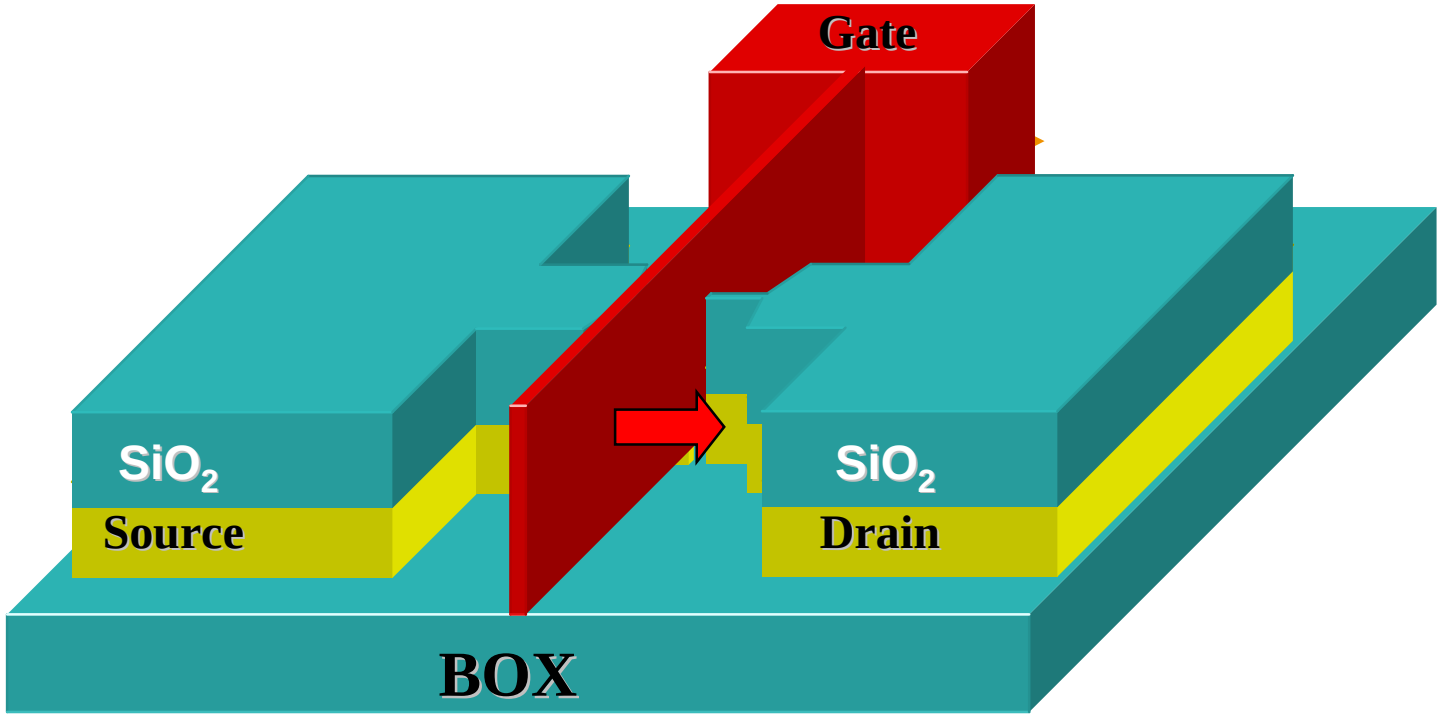
Ultra-Thin Body SOI



Double-Gate SOI MOSFET

Simplified Cross Section of FinFET Double-Gate Device

Courtesy of T-J. King & C. Hu - UC/Berkeley

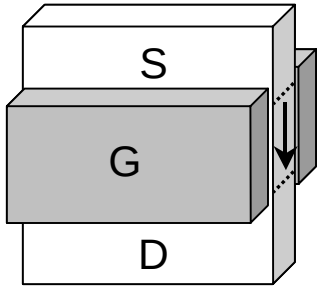


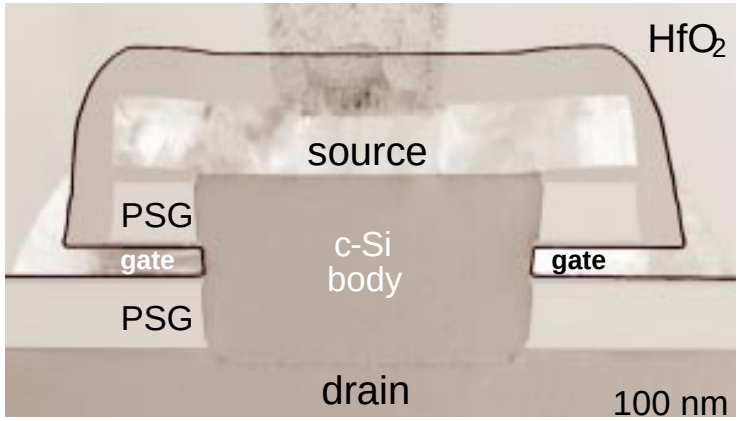
FinFET

Key advantage: relatively conventional processing, largely compatible with current techniques

3-D Transistor Structures

Vertical FET (one type of double-gate MOSFET)

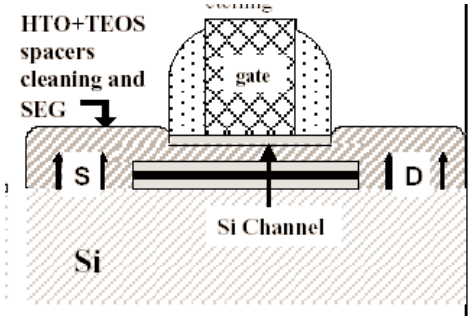


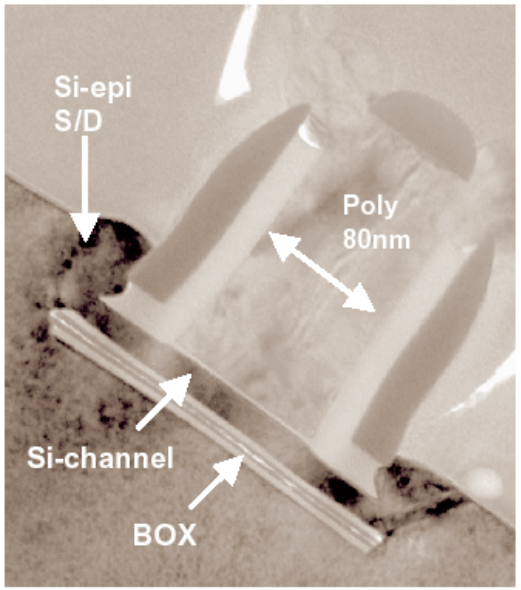


Agere ‘02

REF: Mark Bohr, ECS Meeting PV **2001-2**, Spring, 2001

Silicon on Nothing (SON): localized buried oxide (BOX)





STM ’01

REF: S. Monfray et al., ’01 IEDM, p. 645.

Non-Classical CMOS Summary

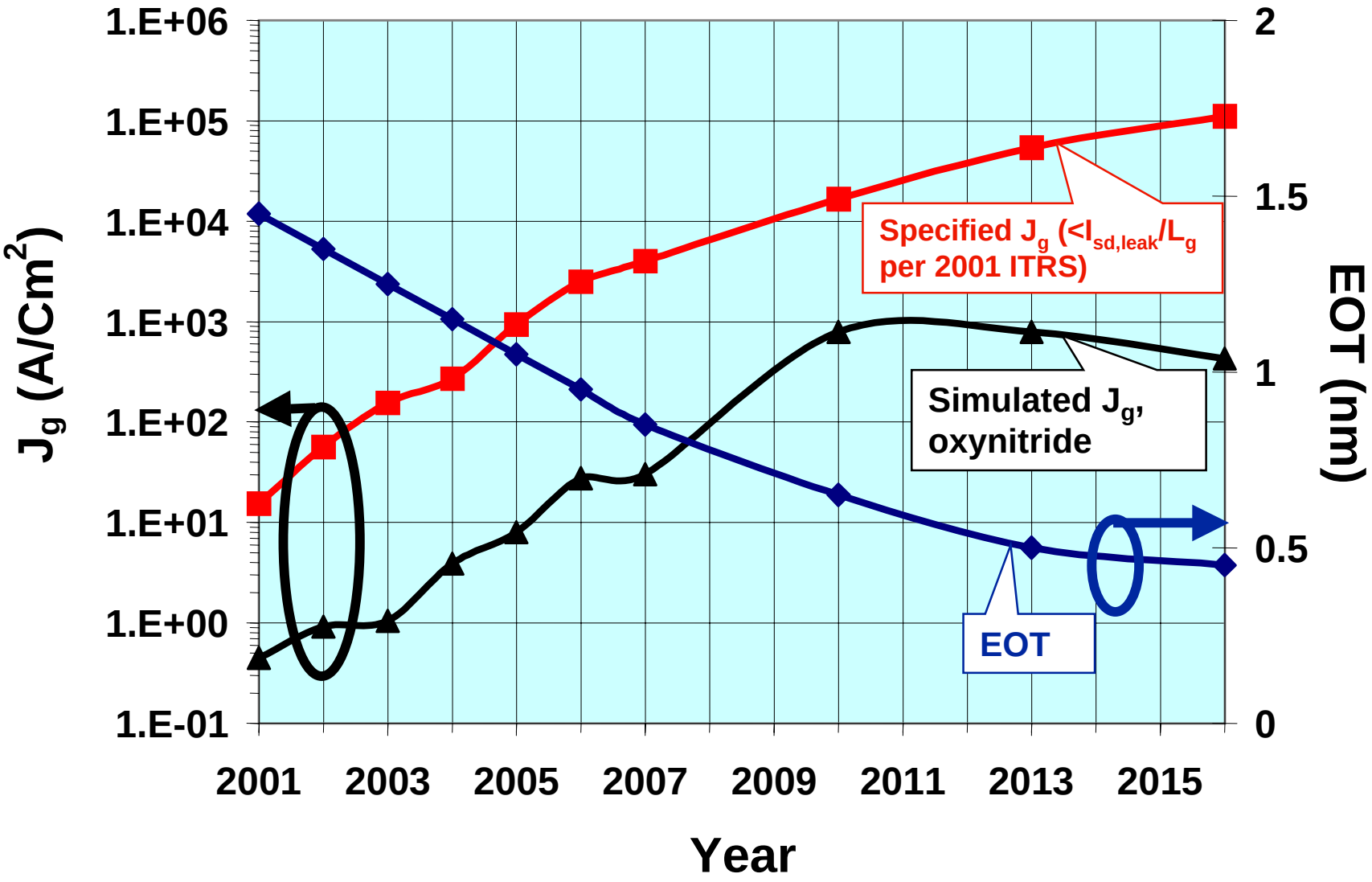
- **Below L_g = 25nm or so, planar bulk CMOS may not scale effectively**
  - **Enhanced mobility will be needed: strained Si on Si-Ge is a potential solution**
  - **Fully depleted ultra-thin body SOI and (preferably) double-gate ultra-thin body MOSFETs are more optimal than planar bulk CMOS. Key issues:**
    - **Effectiveness of planar bulk CMOS scaling in this regime**
      - **Working 15nm devices reported in recent literature**
    - **Finding effective solutions to very difficult processing issues**
  - **Ultimate MOSFET (Lg < 10nm) may be double-gate with high-k, metal gate electrodes, strained Si, etc.**
    - **Such devices will require metal electrodes with near-midgap work functions**

Conclusions

- MOSFET device scaling is the raw material for meeting projected overall chip power, performance, and density requirements
  - Goals/requirements/tradeoffs should be jointly discussed between designers and technologists
  - Considerable design innovation and focus will be required, even with aggressive technology scaling
- Scaling goals vary for different applications
  - High-performance logic driven by transistor speed requirements. Result: high leakage, static power dissipation issues
  - Low-power logic driven by transistor leakage requirements. Result: lower speed than high-performance logic
- Material and process potential solutions include high-k gate dielectric, metal gate electrodes, spike annealing, and eventually, novel S/D annealing and doping
  - High-k needed first for low-power (mobile) chips
- Structural potential solutions: non-classical CMOS
- Structural solutions and material and process solutions being pursued in parallel, and may be combined in the ultimate, end-of-Roadmap device
  - $L_g \leq$ 10nm MOSFETs expected by the end of the Roadmap in 2016
    - For example: L_g~15 and 20nm experimental devices reported in literature and simulations indicate 5nm or less is feasible

Backup Slides

High-Performance Logic: Maximum Gate Leakage Spec's. & Simulations



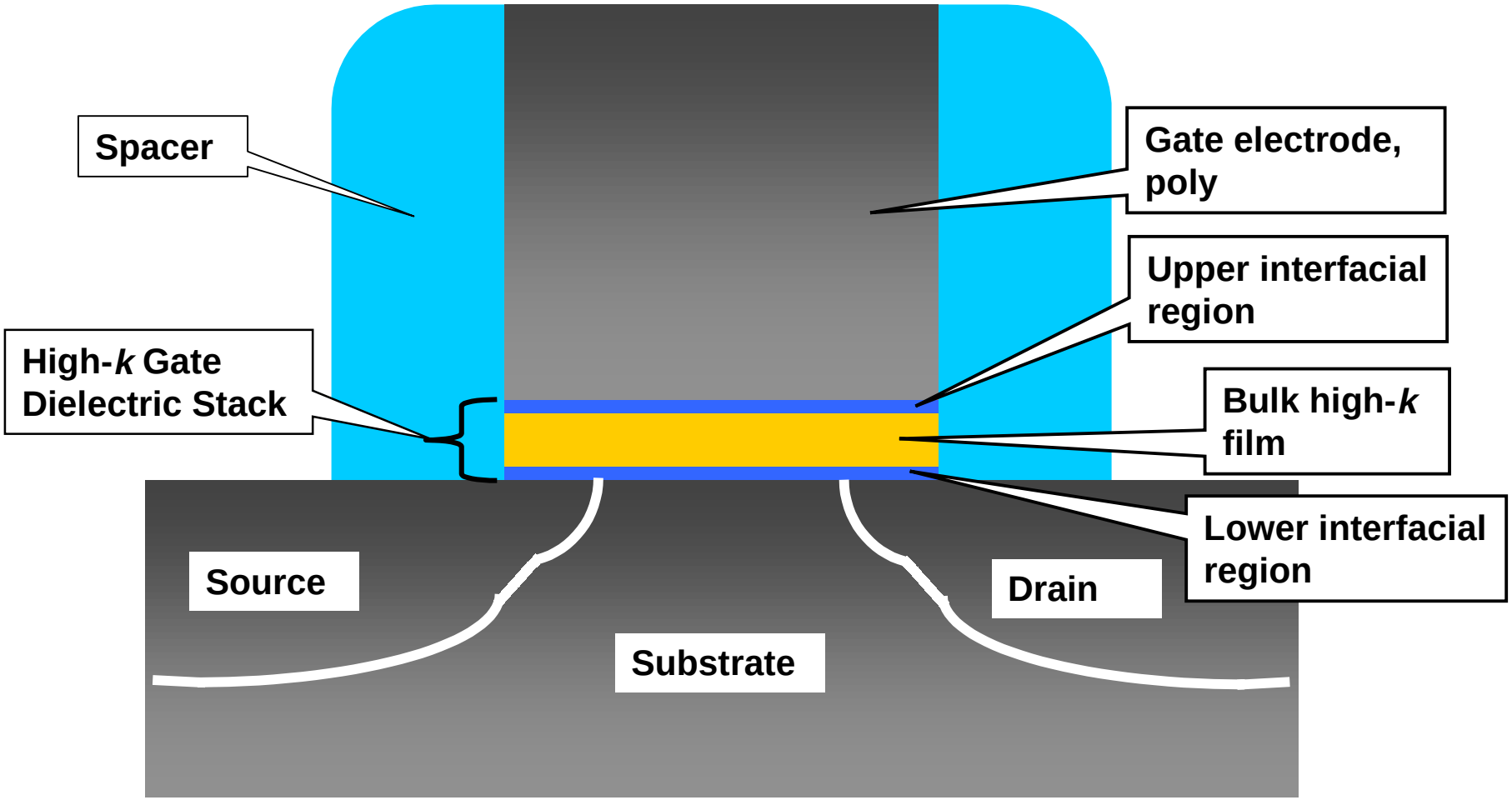
High-Performance Logic Technology Requirements, Data from 2001 ITRS

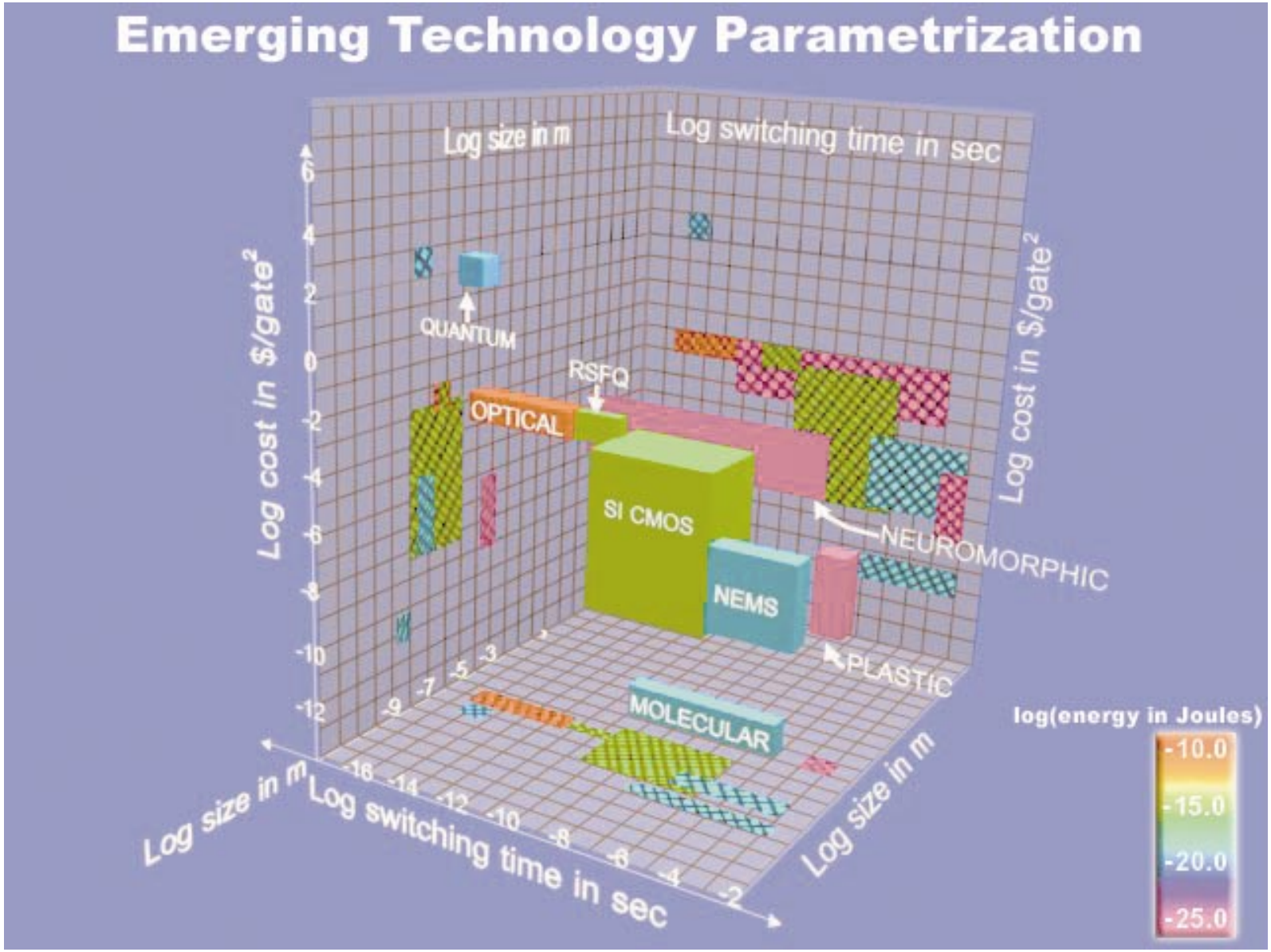
		Near Term							Long Term		
Calendar Year		2001	2002	2003	2004	2005	2006	2007	2010	2013	2016
DRAM half pitch	nm	130	115	100	90	80	70	65	45	32	22
Physical Gate Length, L_g	nm	65	53	45	37	32	28	25	18	13	9
Equivalent oxide thickness, T_{ox}	nm	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1	0.5-0.8	0.4-0.6	0.4-0.5
Nominal Power Supply Voltage (Vdd)	V	1.2	1.1	1.0	1.0	0.9	0.9	0.7	0.6	0.5	0.4
Nominal High-Performance NMOS Sub-Threshold Current (@25C)	uA/um	0.01	0.03	0.07	0.1	0.3	0.7	1	3	7	10
Nominal NMOSFET saturation drive current, I_{on}	uA/um	900	900	900	900	900	900	900	1200	1500	1500
Required Percent Current-Drive "Mobility/Transconductance Improvement"		0%	0%	0%	0%	0%	0%	0%	30%	70%	100%
Parasitic Series S/D resistance, $R_{sd,series}$	ohm-um	190	180	180	180	180	170	140	110	90	80
Parasitic Capacitance Percent of Ideal Gate Capacitance		19%	22%	24%	27%	29%	32%	27%	31%	36%	42%
NMOSFET intrinsic transistor delay, τ_i	ps	1.65	1.35	1.13	0.99	0.83	0.76	0.68	0.39	0.22	0.15
NMOSFET intrinsic transistor switching frequency, $f_i = 1/\tau_i$	GHz	606	742	888	1007	1205	1320	1463	2570	4445	6514
Relative Device Performance		1.0	1.2	1.5	1.6	2.0	2.1	2.5	4.3	7.2	10.7
Energy per (W/Lgate=3) Device Switching Transition (Cgate*(3*Lgate)*V^2)	fJ/Device	0.347	0.212	0.137	0.099	0.065	0.052	0.032	0.015	0.007	0.002
Static Power Dissipation Per (W/Lgate=3) Device	Watts/Device	5.6E-09	6.7E-09	1.0E-08	1.1E-08	2.6E-08	5.3E-08	5.3E-08	9.7E-08	1.4E-07	1.1E-07

Low-Standby-Power (LSTP) Logic Technology Requirements, Data from 2001 ITRS

		Near Term							Long Term		
Calendar Year		**2001**	**2002**	**2003**	**2004**	**2005**	**2006**	**2007**	**2010**	**2013**	**2016**
Technology Node		**130nm**			**90nm**			**65nm**	**45nm**	**32nm**	**22nm**
Physical Gate Length Low-Standby Power (LSTP)	nm	90	80	65	53	45	37	32	22	16	11
Equivalent Physical Oxide Thickness for Low-Standby Power LSTP Tox (EOT)	nm	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	0.9-1.3	0.8-1.2	0.7-1.1
Nominal Low-Standby Power LSTP Power Supply Voltage (Vdd)	V	1.2	1.2	1.2	1.2	1.2	1.2	1.1	1	0.9	0.9
Nominal Low-Standby Power LSTP NMOS Sub-Threshold Current (@25C)	pA/um	1	1	1	1	1	1	1	3	7	10
Nominal Low-Standby Power LSTP NMOS Saturation Current Drive (Idd) (@Vdd, @25C)	uA/um	300	300	300	300	400	400	400	500	600	700
Required Percent Current-Drive "Mobility/Transconductance Improvement"	%	0%	0%	0%	0%	0%	0%	0%	10%	30%	50%
NMOSFET intrinsic transistor switching frequency, $f_i = 1/\tau_i$	GHz	217	227	253	280	398	432	443	700	1096	1522
Energy per (W/Lgate=3) Device Switching Transition (Cgate*(3*Lgate)*V^2)	fJ/Device	0.448	0.381	0.277	0.204	0.163	0.123	0.095	0.047	0.024	0.014
Static Power Dissipation Per (W/Lgate=3) Device	Watts/Device	3.2E-13	2.9E-13	2.3E-13	1.9E-13	1.6E-13	1.3E-13	1.1E-13	2.0E-13	3.0E-13	3.0E-13

Simplified Cross-Section of High K Gate Dielectric Stack




Emerging Technology Parametrization
Log size in m
Log switching time in sec
Log cost in $/gate²
QUANTUM
RSFQ
OPTICAL
SI CMOS
NEMS
NEUROMORPHIC
PLASTIC
MOLECULAR
log(energy in Joules)
-10.0
-15.0
-20.0
-25.0